Notice of Allowability	Application No.	Applicant(s)	
	10/047,772	MARTIN, RUSSEL A.	
	Examiner	Art Unit	
	Jennifer T Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed on 02/02/05*.

2. ☒ The allowed claim(s) is/are *1-42*.

3. ☒ The drawings filed on *02 February 2005* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Von Tersch on 02/27/2005.

1. (Previously Amended) A pixel display circuit comprising: a pixel matrix, the pixel matrix having a first pixel component corresponding to a first color, a second pixel component corresponding to a second color, a third pixel component corresponding to a third color, a fourth pixel component corresponding to the first color, and a fifth pixel component corresponding to the second color, each of the first, second and third pixel components being coupled to a charge storage device and an associated switching device to control activation of each selection of the pixel components, each charge storage device of the first, second and third pixel components receiving a pulse from a previous line prior to activation of the associated switching device, each of the fourth and fifth pixel components being coupled to a charge storage device and an associated switching device to control activation of each selection of the pixel components, each charge storage device of the fourth and fifth pixel components coupled to ground.

2. (Previously Amended) The pixel display circuit of claim 1 in which the switch further comprises a transistor.

3. (Previously Amended) The pixel display circuit of claim 1 in which the switch further comprises a thin film transistor.

4. (Original) The pixel display circuit of claim 1 in which the charge storage device comprises a capacitor.

5. (Original) The pixel display circuit of claim 1 in which the charge storage device comprises a thin film capacitor.

6. (Original) The pixel display circuit of claim 1 in which the first color appears substantially red, the second color appears substantially green and the third color appears substantially blue.

7. (Previously Amended) The pixel display circuit of claim 1 in which each charge storage device of the first, second and third pixel components is fully charged prior to activation of the associated switching device.

8. (Previously Amended) The pixel display circuit of claim 1 wherein the pixel display circuit is coupled to a computing device.

9. (Original) The pixel display circuit of claim 1 wherein the pixel display circuit is coupled to a video signal.

10. (Original) The pixel display circuit of claim 1 wherein the pixel display circuit is coupled to a television signal.

11. (Original) The pixel display circuit of claim 1 wherein the pixel display circuit is coupled to a thin film emissive display device.

12. (Original) The pixel display circuit of claim 1 wherein the pixel display circuit is coupled to a LCD display device.

13. (Presently Amended) An LCD pixel display having a plurality of pixels, each of the pixels having a first plurality of at least three two subpixel elements having paired gate lines, a separate subpixel element, and having a second plurality of at least two subpixel elements, a representative subpixel element of the first plurality comprising:

a capacitor; the capacitor adapted to receive a first control signal; and a switch, the switch adapted to receive a second control signal, the switch being coupled to the capacitor and the switch being coupled to the subpixel element such that the capacitor receives the first control signal before the switch receives the second control signal;

the separate subpixel element comprising:

a capacitor; the capacitor adapted to receive a second control signal; and a switch, the switch adapted to receive a third control signal the switch being coupled to the capacitor and the switch being coupled to the subpixel element such that the capacitor receives the second control signal before the switch receives the third control signal;

and a representative subpixel element of the second plurality comprising:

a capacitor; the capacitor coupled to ground; and a switch, the switch adapted to receive the ~~second~~ third control signal, the switch being coupled to the capacitor and the switch being coupled to the subpixel element.

14. (Original) The LCD pixel display of claim ~~14~~ 13 wherein the first control signal causes a voltage to be applied to one electrode of the capacitor.

15. (Original) The LCD pixel display of claim 14 wherein the second control signal causes the switch to change an optical output associated with the subpixel element.

16. (Original) The LCD pixel display of claim 14 wherein the plurality of pixels form an array and wherein each pixel of the array is coupled to a gate line and a data line such that control signals are transmitted to each switch via the gate line, and wherein the capacitor is coupled to a gate line associated with another pixel.

17. (Presently Amended) An LCD pixel display comprising: a plurality of pixels each pixel further comprising a first plurality of at least three subpixels with an associated paired gate line, wherein each subpixel further comprises a sample and hold circuit wherein a first charging signal is applied prior to ~~the releasing~~ activating the sample and hold circuit;

each pixel further comprising a second plurality of at least two subpixels with an associated gate line, wherein each subpixel further includes a charge storage device coupled to ground and a switch coupled to the associated gate line.

18. (Original) The apparatus of claim 17 above wherein said sample and hold circuit comprises a capacitor transistor arrangement associated with each subpixel and wherein said transistor is timed to open after a previous signal is applied to said capacitor.

19. (Presently Amended) In a pixel array for an LCD display having a plurality of pixels each of ~~said~~ the pixels having a group of subpixels, a first and second of ~~said~~ the subpixels corresponding to a first color, a third subpixel corresponding to a second color and a fourth and fifth subpixel corresponding to a third color comprising:

a first means for switching associated with ~~one of said~~ the first subpixel;

a second means for switching associated with ~~the one of the said~~ the second subpixel;

a third means for switching associated with said the third subpixel;

a fourth means for switching associated with ~~said~~ the fourth subpixel;

a fifth means for switching associated with ~~said~~ the fifth subpixel;

each of ~~said~~ the first, second, third, fourth and fifth switching means having a corresponding means for storing a charge;

~~said~~ the switching means of the first~~, second and third~~ and fourth subpixel being coupled to a first gate line such that each of ~~said~~ the switching means of the first~~, second and third~~ and fourth subpixel is ~~opened~~ closed after each of ~~said~~ the means for storing a charge is charged and in which the gate lines are paired;

the switching means of the ~~fourth~~ second and fifth subpixel being coupled to a second gate line and the storing means of the ~~fourth~~ second, and fifth subpixel being coupled to ground.

20. (Previously Amended) A method for controlling an LCD pixel display having a plurality of pixels, each of the pixels of the plurality of pixels having a first plurality of subpixel elements having paired gate lines and having a second plurality of subpixel elements' having a gate line and a ground line, with a capacitor of each subpixel element of the second plurality of subpixel elements coupled to ground, comprising:

charging a capacitor with a first control signal; and

activating a transistor with a second control signal, the transistor being electrically coupled to the capacitor, and the transistor being coupled to at least one of the first plurality of subpixel elements, such that the capacitor receives the first control signal before the switch receives the second control signal.

21. (Original) The LCD pixel display of claim 20 wherein the first control signal causes a voltage to be applied across the capacitor.

22. (Previously Amended) The LCD pixel display of claim 20 wherein the second control signal causes the transistor to change an optical output associated with one subpixel element of the subpixel elements.

23. (Original) The LCD pixel display of claim 20 wherein the plurality of pixels form an array and wherein each pixel of the array is coupled to a gate line and a data line such that control signals are transmitted to each switch via the gate line, and wherein the capacitor of the first plurality of subelements is coupled to a gate line associated with another pixel.

24. (Original) The LCD pixel display of claim 20 wherein each pixel of the plurality of pixels further comprises a plurality of at least five subpixels with an associated paired gate line, wherein each subpixel further comprises a sample and hold circuit.

25. (Presently Amended) A method for controlling an LCD pixel display having a plurality of pixels, each of the pixels of the plurality of pixels having a first plurality of subpixel elements, a separate subpixel element, a separate subpixel element, and a second plurality of subpixel elements, the LCD display being controlled substantially according to a clock signal, comprising:

charging a capacitor with a first control signal during a first clock period, the first clock period occurring substantially immediately before a second clock period;

activating a transistor with a second control signal during the second clock period, the transistor being electrically coupled to the capacitor, and the transistor being coupled to at least one of the subpixel elements of the first plurality of subpixel elements, the transistor coupling a data signal in the second clock cycle to at least one optical output associated with the at least one of the plurality of subpixel elements,

charging a capacitor of the separate subpixel element with the second control signal during the second clock period;

activating a transistor of the separate subpixel element with a third control signal during a third clock period, the third clock period occurring substantially immediately after the second clock period, the transistor being electrically coupled to the capacitor, the transistor coupling a data signal in the third clock cycle to at least one optical output associated with the separate subpixel element,

activating a transistor with the ~~second~~ third control signal during the ~~second~~ third clock period, the transistor being electrically coupled to a grounded capacitor, the grounded capacitor further coupled to ground, and the transistor being coupled to at least one of the subpixel elements of the second plurality of subpixel elements, the transistor coupling a data signal in the ~~second~~ third clock cycle to at least one optical output associated with the at least one of the plurality of subpixel elements,

transmitting an optical signal from the at least one optical output at least partially in response to the data signal.

26. (Original) The LCD pixel display of claim 25 wherein the first control signal causes a voltage to be applied across the capacitor.

27. (Previously Amended) The LCD pixel display of claim 25 wherein the second control signal causes the transistor to create a potentially visible optical output associated with one subpixel element of the first plurality of subpixel elements.

28. (Previously Amended) The LCD pixel display of claim 25 wherein the plurality of pixels form an array and wherein each pixel of the array is coupled to a first gate line, a second

gate line and a data line, such that the first control signal is received from the first control line coupled to the capacitor, the second control signal is received from the second control line, and the data signal is received from the data line.

29. (Original) The LCD pixel display of claim 25 wherein each pixel of the plurality of pixels further comprises a plurality of at least five subpixels with an associated paired gate line, wherein each subpixel further comprises a sample and hold circuit.

30. (Presently Amended) An apparatus for controlling an LCD pixel display having a plurality of pixels, each of the pixels of the plurality of pixels having a first plurality of subpixel elements having paired gate lines, comprising:

electrical means for charging a capacitor with a first control signal; and

control means for activating a transistor with a second control signal, the transistor being electrically coupled to the capacitor, and the transistor being coupled to at least one of the plurality of subpixel elements, such that the capacitor receives the first control signal before the switch receives the second control signal;

each of the pixels of the plurality of pixels further having a separate subpixel element, comprising:

electrical means for charging a capacitor with the second control signal; and

control means for activating a transistor with a third control signal, the transistor being electrically coupled to the capacitor, and the transistor being coupled to at least one of the plurality of subpixel elements, such that the capacitor receives the second control signal before the switch receives the third control signal;

each of the pixels of the plurality of pixels having a second plurality of subpixel elements, comprising:

a grounded capacitor coupled to ground; and

control means for activating a transistor with ~~a second~~ the third control signal, the transistor being electrically coupled to the capacitor, and the transistor being coupled to. at least one of the plurality of subpixel elements.

31. (Original) The apparatus of claim 30 wherein the electrical means causes a voltage to be applied across the capacitor.

32. (Previously Amended) The apparatus of claim 30 wherein the control means causes the transistor to change an optical output associated with one subpixel element of the first plurality of subpixel elements.

33. (Original) The apparatus of claim 30 wherein each pixel of the plurality of pixels further comprises a plurality of at least five subpixels with an associated paired gate line, wherein each subpixel further comprises a sample and hold circuit.

34. (Presently Amended) An apparatus for controlling an LCD pixel display having a plurality of pixels, each of the pixels of the plurality of pixels having a first plurality of subpixel elements and having a second plurality of subpixel elements, the LCD display being controlled substantially according to a clock signal, comprising:

charging means for charging a capacitor with a first control signal during a first clock period, the first clock period occurring substantially immediately before a second clock period;

activating means for activating a transistor with a second control signal during the second clock period, the transistor being electrically coupled to the capacitor, and the transistor being

coupled to at least one of the first plurality of subpixel elements, the transistor coupling a data signal in the second clock cycle to at least one optical output associated with the at least one of the first plurality of subpixel elements,

the activating means further for activating a transistor with a third ~~second~~ control signal during ~~the second~~ a third clock period, the transistor being electrically coupled to a grounded capacitor, the grounded capacitor being coupled to ground ~~groung~~, and the transistor being coupled to at least one of the second plurality of subpixel elements, the transistor coupling a data signal in ~~the second~~ the third clock cycle to at least one optical output associated with the at least one of the second plurality of subpixel elements,

light emitting means for transmitting an optical signal from the at least one optical output at least partially in response to the data signal.

35. (Original) The apparatus of claim 34 wherein the charging means causes a voltage to be applied across the capacitor.

36. (Previously Amended) The apparatus of claim 34 wherein the activating means causes the transistor to create a potentially visible optical output associated with one subpixel element of the first plurality of subpixel elements.

37. (Previously Amended) The apparatus of claim 34 wherein the plurality of pixels form an array and wherein each pixel of the array is coupled to a first gate line, a second gate line and a data line, such that the first control signal is received from the first control line coupled to the capacitor, the second control signal is received from the second control line, and the data signal is received from the data line

38. (Original) The apparatus of claim 34 wherein each pixel of the plurality of pixels further comprises a plurality of at least five subpixels with an associated paired gate line, wherein each subpixel further comprises a sample and hold circuit.

39. (Presently Amended) An LCD pixel display having a plurality of pixels, each of the pixels having a first plurality of at least ~~three~~ two subpixel elements having paired gate lines, and having a second plurality of at least two subpixel elements having, a representative subpixel element of the first plurality comprising:

a storage means; the storage means adapted to receive a first control signal; and

a switch means, the switch means adapted to receive a second control signal, the switch means coupled to the storage means and the switch means being coupled to the subpixel element such that the storage means receives the first control signal before the switch means receives the second control signal;

a representative subpixel element of the second plurality comprising:

a grounded storage means; the storage means coupled to ground; and

a switch means, the switch means adapted to receive a third ~~second~~ control signal, the switch means coupled to the storage means and the switch means being coupled to the subpixel element.

40. (Original) The LCD pixel display of claim 39 wherein the first control signal causes a voltage to be applied to the storage means.

49. (Original) The LCD pixel display of claim 39 wherein the second control signal causes the switch means to change an optical output associated with the subpixel element.

42. (Original) The LCD pixel display of 39 wherein the plurality of pixels form an array and wherein each pixel of the array is coupled to a gate line and a data line such that control signals are transmitted to the switch means via the gate line, and wherein the storage means is coupled to a gate line associated with another pixel.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer T Nguyen whose telephone number is 571-272-7696. The examiner can normally be reached on Mon-Fri: 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edouard Patrick can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JNguyen
03/03/2005

REGINA LIANG
PRIMARY EXAMINER